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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,346	09/25/2003	Shih-Lung Chen	0941-0843P	6597

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,346	CHEN ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10 and 14-22, drawn to a method of forming integrated circuit device, classified in class 438, subclass 100+.

II. Claims 11-13 and 23-24, drawn to semiconductor integrated circuit device, classified in class 257, subclass 301.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another materially different process for example in claim 1, forming two access transistors first on the substrate outside a region where a pair of neighboring trenches are going to be formed and then forming the pair of neighboring trenches instead of providing a substrate having a pair of neighboring trenches and forming the two access transistors. Furthermore, the product as claimed can be made by another materially different process for example in claim 14, forming the top plate and the conductive layer at the same time instead of forming the top plate first and then forming the conductive layer later.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

6. During a telephone conversation with Joe Muncy on 8/13/2004 a provisional election was made with traverse to prosecute the invention of group I claims 1-10 and 14-22. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-13 and 23-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "below the surface of the substrate" as recited in claims 1 and 14 in lines 12-13 is unclear. The substrate has both upper and lower surfaces. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 7, 10, 14 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hieda et al., US patent No. 5,736,760.

Regarding claim 1, Hieda teaches (fig. 34B) providing a substrate (124) having a pair of neighboring trenches (56); forming a buried trench capacitor (126,72 and 70a,) in a lower portion of each trench (56); forming an asymmetric collar insulating layer (170), having a high level portion (region of 170 on left side of the trench) and a low level portion (region of 170 on right side of the trench), over an upper portion of the sidewall of each trench, and forming a conductor layer (70b and 168a), overlying the buried trench capacitor in each trench, below the surface of the substrate (124) with a lower part of the conductive layer surrounded by the asymmetric collar insulating layer, wherein the high level portion of the asymmetric collar insulating layer is adjacent to the substrate between the neighboring trenches and the low level portion (collar oxide on left side is covered by 168a) is covered by an upper part of the conductive layer (168a); forming a dielectric layer (80) overlying the conductive layer (168a) in each trench; and

forming two access transistors (transistors defined by region 60, 74 and 76) on the substrate outside of the pair of the neighboring trenches, respectively, wherein the two access transistors have source/drain regions (74 and 76) electrically connecting to the conductive layer (fig. 34B).

The limitation of "a method for forming a volatile memory structure" is not given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 7, Hieda teaches the entire claimed process of claim 1 above including the conductive layer (70b) is a doped polysilicon layer (col. 26, lines 19-35).

Regarding claim 10, Hieda teaches the entire claimed process of claim 1 above including forming a gate (60) on the dielectric layer over each trench.

Regarding claims 14 and 20, Hieda teaches substantially the entire claimed process of claims 1 and 7 above including forming a buried bottom plate (126) in the substrate around a lower portion of the trench; forming a capacitor dielectric layer (72) over a lower portion of the sidewall of the trench; forming a top plate (70a) in the trench and surrounded by the capacitor dielectric layer (fig. 34B).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-6, 8-9, 15-19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda in view of Kenny US patent No. 4,801,988.

Regarding claim 2, Hieda teaches substantially the entire claimed process of claim 1 above except explicitly stating forming a first conductive layer overlying the buried trench capacitor in each trench and surrounded by an insulating spacer protruding the surface of the first conductive layer; covering portions of the insulating spacers adjacent to the substrate between the neighboring trenches by a masking layer; removing the uncovered insulating spacers to form the asymmetric collar insulating layer in each trench; removing the masking layer; and forming a second conductive layer overlying the first conductive layer, wherein the first conductive layer and the second conductive layer are combined as the conductive layer.

The above process step is conventional in the art and is also taught by Kenny (figs. 3A-3H), where a first conductive layer (fig. 3D) overlying the buried trench capacitor in the trench (560) and surrounded by an insulating spacer (340 and 360) protruding the surface of the first conductive layer (fig. 3E); covering portions of the insulating spacers adjacent to the substrate by a masking layer (700); removing the uncovered insulating spacers to form the asymmetric collar insulating layer (340 and

360 are no more symmetric) in the trench; removing the masking layer (fig. 3G); and forming a second conductive layer (800) overlying the first conductive layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process step of forming the asymmetric oxide layer taught by Kenny in the process of Hieda in order to facilitate the construction of densely packed arrays of trench capacitors.

Regarding claim 3, Hieda teaches substantially the entire claimed process of claim 1 above including the masking layer is a photoresist layer (700).

Regarding claim 4, Hieda teaches substantially the entire claimed process of claims 1 and 2 above including forming a sacrificial layer (550) and removing the sacrificial layer and the masking layer (fig. 3F).

Regarding claim 5, Hieda teaches substantially the entire claimed process of claims 1 and 2 above including the sacrificial layer (550) is anti-reflection layer. Since layer (550) is an oxide layer and since an oxide layer is conventionally used as anti-reflection layer, layer (550) is capable of serving as an anti-reflection layer.

Regarding claim 6, Hieda teaches substantially the entire claimed process of claims 1 and 2 above including the masking layer is a photoresist layer (700).

Regarding claim 8, Hieda teaches (fig. 34B) the entire claimed process of claim 1 above including before the step of forming the dielectric layer, further comprises: forming active area/isolation areas through an active area masking layer.

Since the combined process of Hieda and Kenny includes the step of using the masking layer (700) and since Hieda further teaches the use of isolation structure (68)

separating the active regions of the transistors, the combined process of Hieda and Kenny is capable of forming active area/isolation area using the masking layer (700).

Regarding claim 9, Hieda teaches the entire claimed process of claims 1 and 8 above including the active area-masking layer is a strap type pattern.

Regarding claims 15-17-19, 21 and 22 Hieda teaches substantially the entire claimed process of claims 1-5, 6, 8-9 and 14 above including the masking layer is a photoresist layer (700).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-E are cited as being related to trench capacitor. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
August 31, 2004

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